UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/710,891 | 08/11/2004 | Yuan-Ting Wu | MTKP0088USA | 4890 |

27765 7590 08/02/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

| EXAMINER | |
|---|---|
| NGUYEN, CAMVAN T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2192 | |

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/710,891 | WU ET AL. | |
| | Examiner | Art Unit | |
| | CamVan T. Nguyen | 2192 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *8/16/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 8 – 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claims 8-13 recites the limitation "device". There is insufficient antecedent basis for this limitation in the claim. For purpose of examination the "device" will be construed as the "microprocessor system" of claim 7.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaiser et al (U.S. Patent No. 5,784,710).

a. For claim 1, a method for accessing a memory to protect a memory section from being accessed or changed incorrectly when accessing the memory comprising: (a) generating a first logic

address data (figure 2, ADDRESS (N-M); column 3, lines 56-58); (b) selectively outputting the first logic address data or a second logic address data as a physical address data by using an address translator according to a control signal (figure 2, input 0 of MUX 205 = first logic address data, input 1 of MUX 205 = second logic address data, NEW ADDRESS (N-M) = physical address data, circuitry 20 = address translator, SELECT = control signal; column 4, lines 21-24); and (c) accessing the memory according to the physical address data (column 4, lines 25-28 & 31-33); wherein the second logic address data is a result obtained after operating the first logic address data (figure 2, OR 202; column 4, lines 9-11).

b. For claim 2, the method of claim 1 wherein Step (b) further comprises operating the first logic address data by using the address translator according to a setup value in order to generate the second logic address data (figure 2, ADDRESS MASK (N-M) = setup value; column 4, lines 9-11).

c. For claim 3, the method of claim 2 wherein the setup value is a value representing a characteristic of the memory section (column 3, line 67 – column 4, line 2; column 4, lines 5-8).

d. For claim 4, the method of claim 2 wherein the setup value is stored in a register (it is inherent that the ADDRESS MASK (N-M) has to be buffered in a register in order for it to be fed to the OR gate 202).

e. For claim 5, the method of claim 2 wherein the address translator further comprises an operating unit (figure 2, OR 202), and Step (b) further comprises operating the first logic address data by using the operating unit according to the setup value to generate the second logic address data (figure 2, ADDRESS MASK (N-M) *OR*ed with ADDRESS (N-M) = input 1 of MUX 205).

f. For claim 6, the method of claim 2 wherein the address translator further comprises a multiplexer (figure 2, MUX 205), and Step (b) further comprises multiplexing the first logic address data and the second logic address data by using the multiplexer to selectively output the first logic address data or the second logic address data (figure 2, MUX 205, input 0 = first logic address data, input 1 = second logic address data).

g. For claim 7, a microprocessor system for accessing a memory comprising: a microprocessor (figure 1) for providing a first logic address data (figure 2, ADDRESS (N-M)); a memory comprising a first memory section (figure 2, IPL 105 & ROM 104) and a second memory section (figure 1, memory 102); and an address translator coupled between the microprocessor and the memory (figure 1, circuitry 20) to selectively output the first logic address data or a second logic address data as a physical address data (figure 2; MUX 205); wherein the second logic address data is a result obtained after operating the first logic address data (figure 2, OR

202) and the microprocessor accesses data of the first memory section or the second memory section according to the physical address data (column 4, lines 9-28, either memory 102 or memory on I/O bus 106 will be accessed).

h. For claim 8, the device (system) of claim 7 wherein the memory is a non-volatile memory (figure 2, IPL 105 & ROM 104)

i. For claim 9, the device (system) of claim 7 wherein the address translator operates the first logic address data (figure 2, ADDRESS (N-M)) according to a setup value (figure 2, ADDRESS MASK (N-M) 201) to generate the second logic address data (figure 2, input 1 of MUX 205 = second logic address data; column 4, lines 9-11).

j. For claim 10, the device (system) of claim 9 wherein the setup value is a value representing a characteristic of the first memory section (column 3, line 63 – column 4, line 2; column 4, lines 5-8).

k. For claim 11, the device (system) of claim 9 wherein the address translator further comprises an operating unit (figure 2, OR 202) to operate the first logic address data according to the setup value in order to generate the second logic address data (figure 2, ADDRESS MASK (N-M) *OR*ed with ADDRESS (N-M) = input 1 of MUX 205).

l. For claim 12, the device (system) of claim 9 wherein the address translator further comprises a register for storing the setup value (it is inherent that the ADDRESS MASK (N-M) has to be buffered in a register in order for it to be fed to the OR gate 202).

m. For claim 13, the device (system) of claim 7 wherein the address translator further comprises a multiplexer (figure 2, MUX 205) for multiplexing the first logic address data (ADDRESS (N-M)) and the second logic address data (output of OR 202) in order to selectively output the first logic address data or the second logic address data.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Chuang et al. (U.S. 2004/0172515 A1) teaches the claimed invention: A microprocessor system for accessing a memory comprising: a microprocessor for providing a first logic address data; a memory comprising a first memory section and a second memory section, and an address translator coupled between the microprocessor and the memory to selectively output the first logic address data or a second logic address data as a physical address data; wherein the second logic address data is a result obtained after operating the first logic address data and the microprocessor accesses data of the first memory section or the second memory section according to the physical address data. The memory is a

non-volatile memory. The address translator operate the first logic address data according to a setup value to generate the second logic address data, wherein the setup value is a value representing a characteristic of the first memory section. The address translator further comprises an operating unit to process the first logic address data according to the setup value in order generate the second logic address data. The address translator further comprises a register for storing the setup value. The address translator comprises a multiplexer for multiplexing the first logic address data and the second logic address data in order to selectively output the first logic address data or the second logic address data.

b. Tseng et al. (U.S. Patent Pub. No. 2004/0186944) teaches a microprocessor system having a plurality of memory banks, a memory bank control circuit, and a multiplexer for outputting a page selection signal.

c. Shimomura (U.S. Patent No. 6,578,132 B1) teaches an address processing circuitry which includes calculating circuitry capable of outputting a $2^{nd}$ address data by performing calculation on at least a portion of the $1^{st}$ address data, and a selector which outputs the $2^{nd}$ address data when a control signal is applied and outputs the $1^{st}$ address data when the control signal is not applied.

d. Sheriff et al. (U.S. 2005/0144417 A1) teaches a technique to manage multiple-mapped memory and to selectively execute at least a

portion of a process from either an unprotected function or a protected function.

e. Zhou et al. (U.S. Patent No. 5,913,924) teaches a computer system which includes a number of storage elements encoded with space selection instructions.

f. Dayan et al. (U.S. Patent No. 5,187,792) teaches an apparatus and method for reclaiming a portion of random access memory.

g. Ahn (U.S. Patent No. 6,564,283 B1) teaches a microprocessor capable of functioning in an expanded address mode.

h. Bauer (U.S. Patent No. 4,716,586) teaches a state sequence dependent read only memory.

i. Chou (U.S. Patent No. 6,785,798 B2) teaches an apparatus that generates address for circular address buffers in memory, in which a higher boundary of a circular buffer is implied from the current address.

j. Riedlinger et al. (U.S. Patent No. 6,446,187 B1) teaches virtual address bypassing using a local page mask.

k. Hansen et al. (U.S. Patent No. 5,909,703) teaches a method and apparatus for banking addresses for DRAMs.

l. Dey et al. (U.S. Patent No. 5,893,932) teaches an address path architecture.

m. DeRoo et al. (U.S. Patent No. 5,822,601) teaches an apparatus to allow a cpu to control the relocation of code blocks for other cpus.

***Examiner's Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CamVan T. Nguyen whose telephone number is 571-270-1039. The examiner can normally be reached on Monday-Thursday 8:30am - 6:00pm; alternate Friday 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Robertson can be reached on 571-272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CN
CamVan Nguyen
7/24/2006

DAVID ROBERTSON
SUPERVISORY PATENT EXAMINER